• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It is suitable for automotive application.

• Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching

■Low Thermal resistance

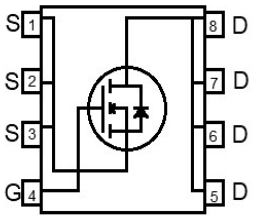
•Application

■BLDC Motor driver

■DC-DC

■Battery protection

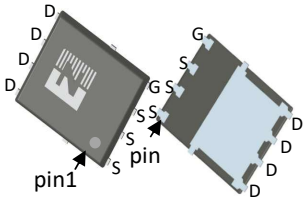
• Product Summary



V_{DS}= 40V

$R_{DS(ON)}$ = 5.5mΩ

I_D= 68A



DFN5*6

RoHS

REACH COMPLIANT

HF

•Ordering Information:

Part NO.	ZMSA055N04HN
Marking	ZMS055N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

•Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage①	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	68	A
	I_D	T_C=75℃	63	A
	I_D	T_C=100℃	55	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	272	A
Total Power Dissipation	P_D	T_C=25℃	71	W
Total Power Dissipation	P_D	T_A=25℃	3.0	W
Operating Junction Temperature	T_J		-55 to +175	℃
Storage Temperature	T_{STG}		-55 to +175	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	40	mJ
		L=0.5mH, V_{GS}=10V, Rg=25Ω,	84	mJ
ESD Level (HBM)			CLASS 1B	

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.1	°C/W
Thermal resistance, junction-ambient	R_{thJA} ②		-	50	°C/W
Soldering temperature (total time<10s)	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	2.0	2.7	4.0	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 40V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 14A		5.5	6	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V, I_{SD} = 4A		7		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 14A			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	908	-	pF
Output capacitance	Coss		-	244	-	
Reverse transfer capacitance	Crss		-	10	-	
Gate Risistance	Rg	f = 1MHz	-	1.2		Ω
Total gate charge	Qg	V_{DD} = 25V, I_D = 14A, V_{GS} = 10V	-	17.1	-	nC
Gate - Source charge	Qgs		-	3.5	-	
Gate - Drain charge	Qgd		-	5.8	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	5	-	ns
Turn-ON Rise time	t_r		-	10	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	8	-	ns
Turn-Off Fall time	t_f		-	3	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=20V, dI_S/dt = 100A/us, I_S=50A	-	30	-	ns
Reverse Recovery Charge	Q_{RR}		-	21	-	nC

Fig.1 Gate-Charge Characteristics

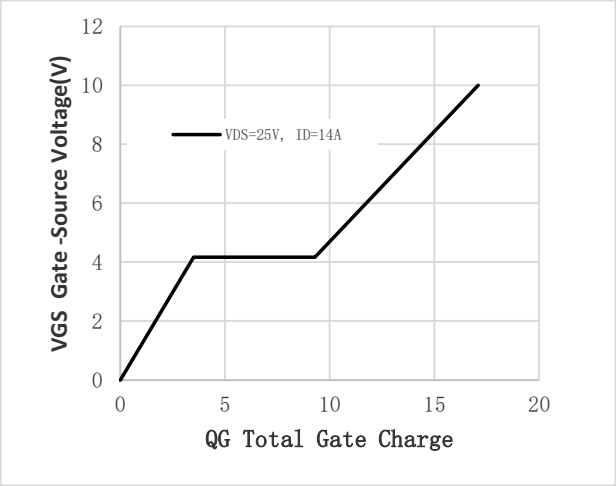


Fig.2 Capacitance Characteristics

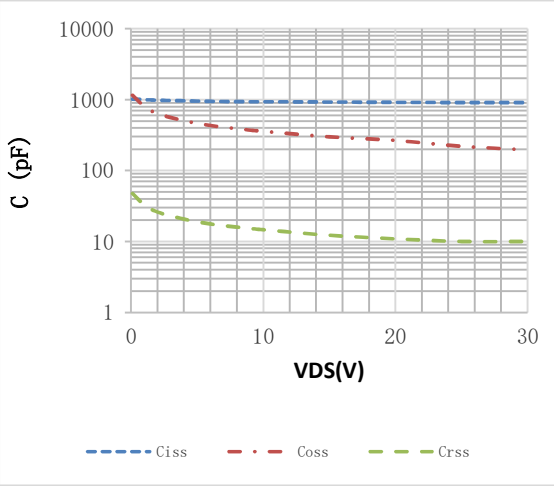


Fig.3 Power Dissipation

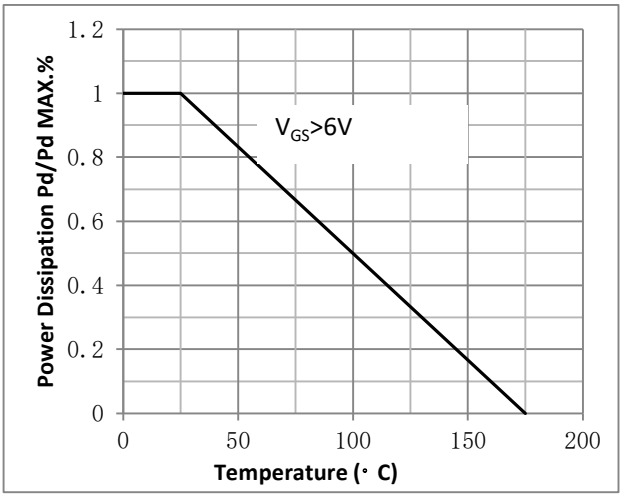


Fig.4 Typical output Characteristics

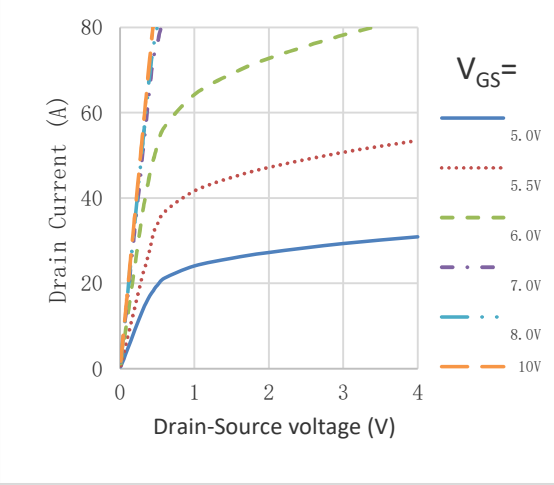


Fig.5 Threshold Voltage V.S Junction Temperature

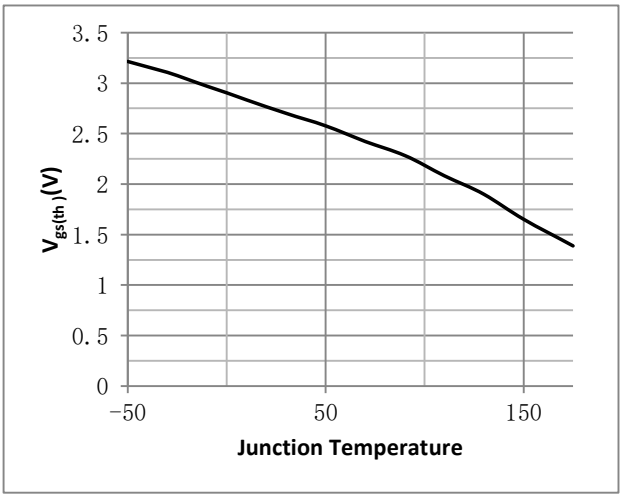


Fig.6 Resistance V.S Drain Current

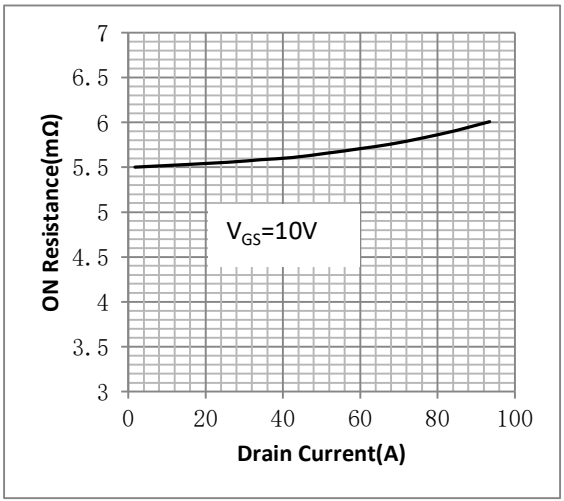


Fig.7 On-Resistance VS Gate Source Voltage

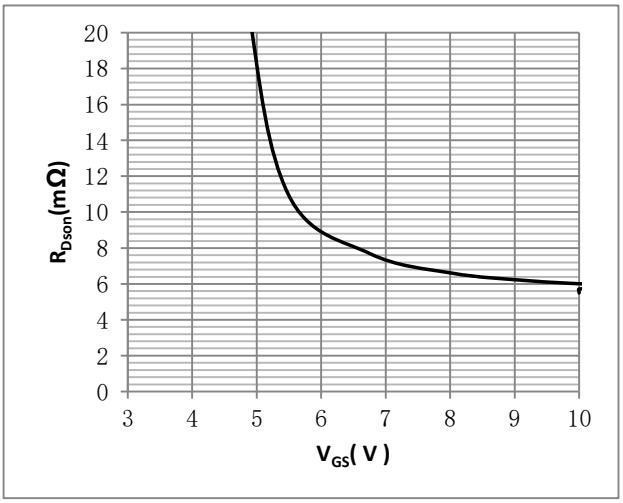


Fig.8 On-Resistance V.S Junction Temperature

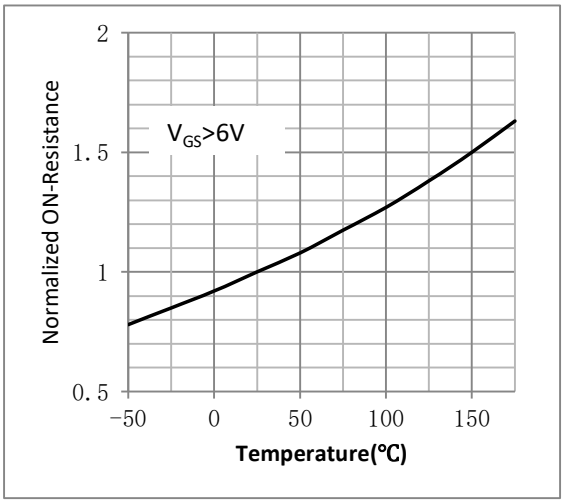


Figure 9. Diode Forward Voltage vs. Current

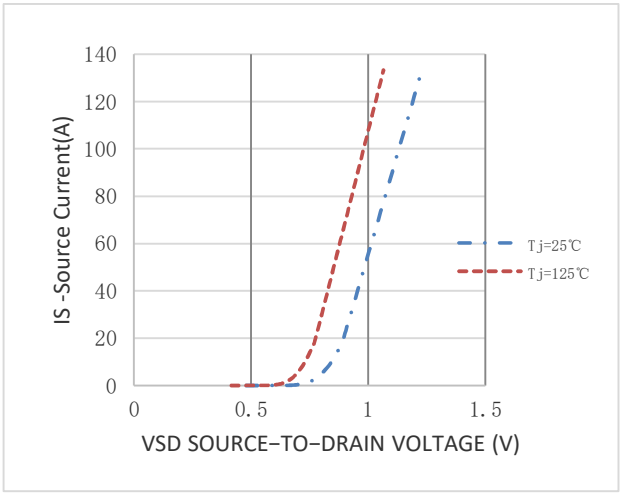


Figure 10. Transfer Characteristics

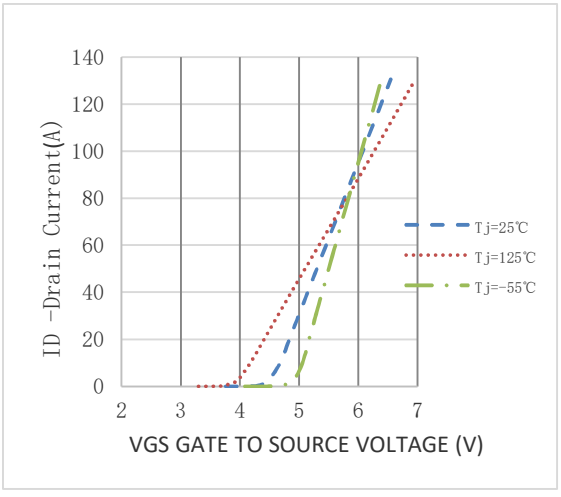


Fig.11 Safe Operating Area

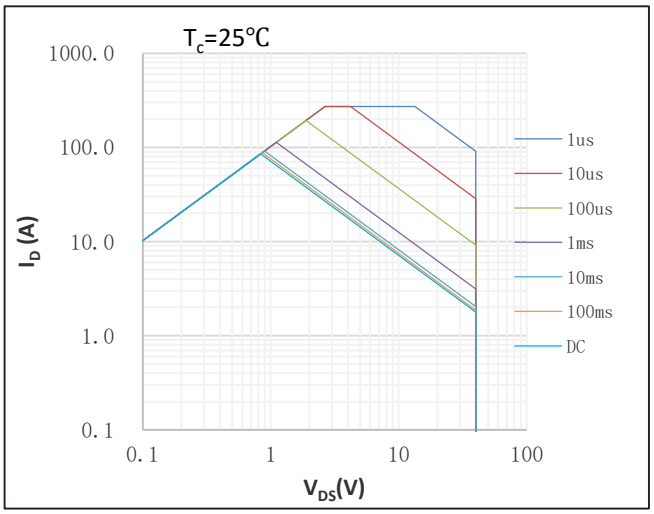


Fig.12 ID vs. Junction Temperature③

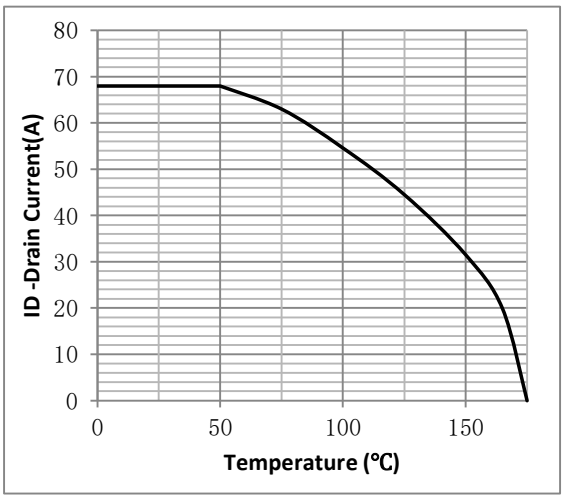
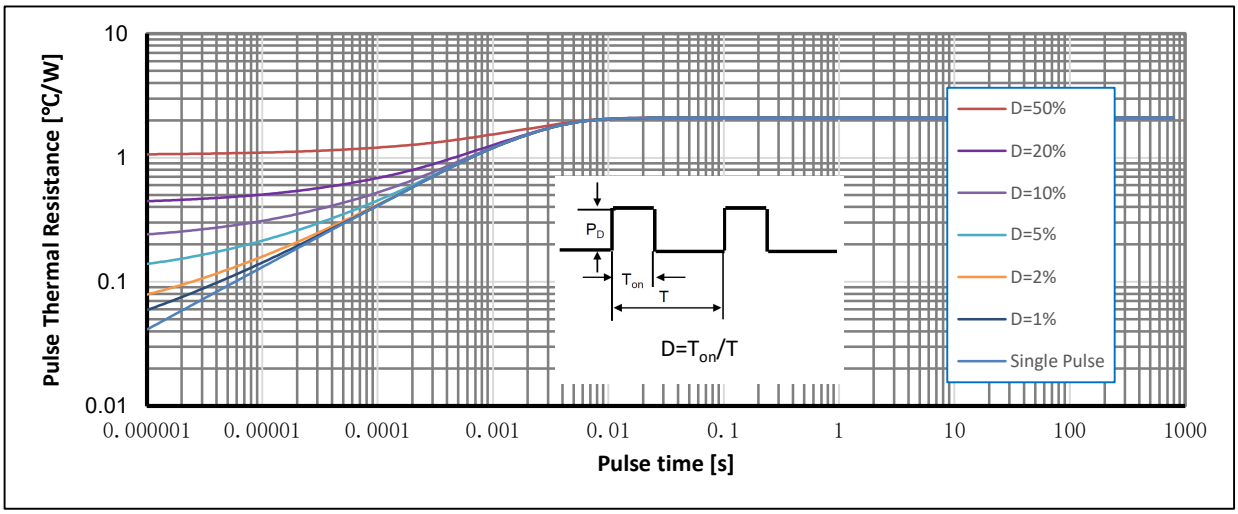
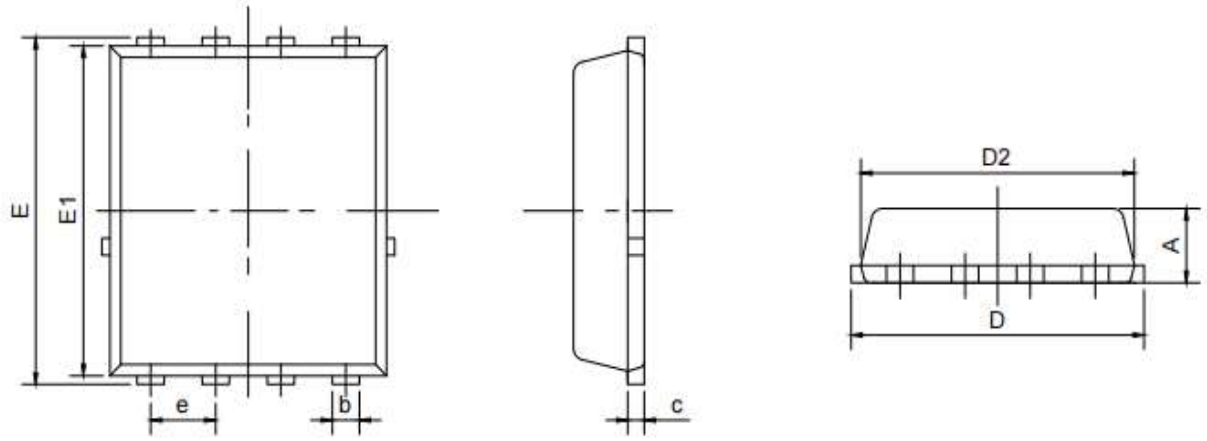


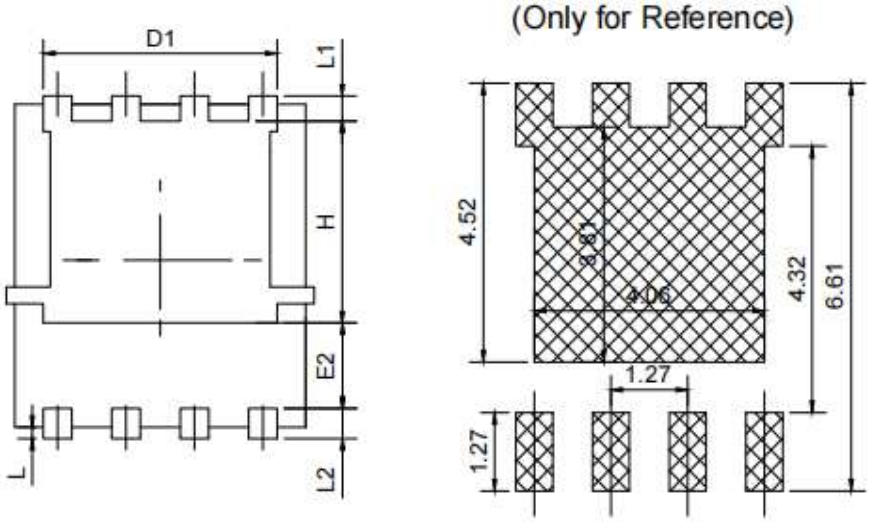
Fig.13 Transient thermal impedance from junction to case as a function of pulse duration; max values



●DFN5*6 Package Outline

1	WPOD008	DFN5*6 SINGLE PACKAGE OUTLINE SPEC
REV	DRAWING NUMBER	TITLE





SYMBOLS	COMMON	
	UNIT: mm	
	MIN.	MAX.
A	0.90	1.17
b	0.30	0.51
c	0.15	0.35
D	4.80	5.40
D1	4.00	4.40
D2	4.80	5.00
E	5.90	6.25
E1	5.65	5.85
E2	1.10	-
e	1.27BSC	
L	0.05	0.25
L1	0.28	0.65
L2	0.38	0.71
H	3.30	3.90

Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. V_{GS}=10V.

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Revision History

Version	Date	Change
A	2022.1.6	
B	2022.2.26	1.Add Dynamic characteristic tf，tr etc.
C	2022.9.5	1.Add Reach,HF figure,2.ID modify
D	2022.9.19	Change dimension A,L
E	2023.12.19	Correct SOA
F	2024.2.28	Correct package outline dimension
G	2024.8.30	Modified Rdson up limit, id@75℃,100℃
H	2025.1.16	Correct SOA
H1	2025.7.23	1. Add 1us SOA curve 2. Add transient thermal impendence curve
I	2025.12.15	Modify Qg value and chart
J	2026.3.14	Modify ESD level.